IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	
Wagh *et al.*	Examiner: Richard Franklin
Serial No.: 10/815,347	Art Unit: 2181
Filed: March 31, 2004	Confirmation No.: 8283
For: APPARATUS AND METHOD TO MAXIMIZE BUFFER UTILIZATION IN AN I/O CONTROLLER	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Appellants submit the following Appeal Brief pursuant to 37 C.F.R. §41.37(c) for consideration by the Board of Patent Appeals and Interferences. The Appellants authorize the amount of $510.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(f) to be charged to Deposit Account No. 02-2666.

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I. REAL PARTY IN INTEREST

Mahesh U. Wagh, Wilfred W. Kwok, and Sridhar Muthrasanallur, the parties named in the caption, transferred their rights to the subject Application through an assignment recorded on March 31, 2004 (Reel/Frame 015180/0393) to Intel Corporation, of Santa Clara, California, United States. Thus, as the owner at the time the brief is being filed, Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, be directly affected by or have a bearing on the Board's decision in this Appeal.

III. STATUS OF CLAIMS

Claims 1-27 are pending, and claims 8-19 and 25-27 are rejected in the Application. Claims 1-7 and 20-24 are withdrawn from consideration. The Appellants respectfully appeal the rejection of claims 8-19 and 25-27.

IV. STATUS OF AMENDMENTS

Amendments were submitted after the Final Office Action mailed on August 21, 2007. Two new additional claims were presented, but were denied entry in the Advisory Action mailed October 29, 2007. No other amendments were submitted after the mailing of the Final Office Action.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 8 recites a method comprising: determining an amount of available memory credits in an input/output (I/O) controller communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits (*See* pg. 2, ll. 16-22; pg. 7, ll. 4-14; pg. 12, ll. 29-30; pg. 13 ll. 1-4; Fig. 1, item 130; Fig. 4, item 420); and sending an amount of data from the chipset to the I/O controller, the amount of data sent being one of equivalent to or less than the communicated available memory credit amount (*See* pg. 2, ll. 16-22; pg. 7, ll. 4-14; pg. 12, ll. 29-30; pg. 13 ll. 1-4; Fig. 1, item 130; Fig. 4, item 420).

Claim 14 recites the method of claim 13, wherein temporarily storing the data in at least one buffer comprises: storing the data in a plurality of buffers (*See* pg. 5, ll. 15-20; pg. 13, ll. 11-13; Fig. 2, items 230, 240; Fig. 4, item 440).

Claim 19 recites the method of claim 18, wherein keeping track of the number of memory credits comprises: simultaneously keeping track of amounts of memory credits the I/O controller empties onto the I/O bus, amounts of memory credits sent to the I/O controller and amounts of memory credits made available by distribution of data sent from the chipset to a plurality of buffers contained within the I/O controller (*See* pg. 9, ll. 3-32 to pg. 10, ll. 1-3; pg. 13, ll. 27-31; pg. 14, ll. 1-4).

Claim 25 recites a machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising: determining an amount of available memory credits in an input/output (I/O) controller (*See* pg. 4, ll. 30-31; pg. 5, ll. 1-5; pg. 6, ll. 1-24; pg. 12, ll. 22-28; Fig. 1, item 140; Fig. 2, item 200; Fig. 4, item 410); communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits (*See* pg. 2, ll. 16-22; pg. 7, ll. 4-14; pg. 12, ll. 29-30; pg. 13 ll. 1-4; Fig. 1, item 130; Fig. 4, item 420); and sending an amount of data from the chipset to the I/O controller, the amount of data sent being one of equivalent to or less than the communicated available memory credit amount (*See* pg. 2, ll. 16-22; pg. 7, ll. 4-14; pg. 12, ll. 29-30; pg. 13 ll. 1-4; Fig. 1, item 130; Fig. 4, item 420).

Claim 27 recites the machine read medium of claim 26, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising: temporarily storing the data in at least one buffer contained within the I/O controller (*See* pg. 4, ll. 9-14; pg. 5, ll. 13-25; Fig. 2, items 200, 240; Fig. 4, item 440); emptying the buffer of at least some of the data temporarily stored in the I/O controller onto an I/O bus coupled to the I/O controller to create a new amount of available memory credits in the I/O controller (*See* pg. 4, ll. 9-14; pg. 5, ll. 26-30; pg. 13, ll. 13-20; Fig. 1, items 150, 160; Fig. 4, item 450); and simultaneously tracking amounts of memory credits the I/O controller empties onto the I/O bus,

amounts of memory credits sent to the I/O controller from the chipset and amounts of memory credits made available by distribution of the data sent from the chipset to a plurality of buffers contained within the I/O controller (*See* pg. 9, ll. 3-32; pg. 10, ll. 1-3; pg. 13, ll. 27-31; pg. 14, ll. 1-4).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 8 and 25 stand rejected under 35 U.S.C. §103(a) as being obvious over Good *et al.* (US 6,240,095 B1), in view of Shimojo *et al.* (US 5,787,072). Claims 9, 12-19, and 26-27 stand rejected under 35 U.S.C. §103(a) as being obvious over Good *et al.*, in view of Shimojo *et al.*, and further in view of Collier *et al.* (US 2002/0150049 A1). Claims 10 and 11 stand rejected under 35 U.S.C. §103(a) as being obvious over Good *et al.*, in view of Shimojo *et al.*, and further in view of Collier *et al.* and Anderson (US 2003/0223369 A1).

All of the claims do not stand or fall together. The basis for the separate patentability of the claims is set forth below.

VII. ARGUMENT

A. Overview of the Cited References

1. Good *et al.*

Good *et al.* involves a buffer memory interface that is interposed between a network device (*e.g.*, a remote server) and a host device (*e.g.*, a local computer) for the management of data transmission. The buffer memory interface manages data according to two levels of buffering. One level of buffering (the input buffer and the output buffer) maintains the actual data being transmitted, and the other level of buffering (the receive buffer and the command buffer) maintains instructions relating to the data. This buffer memory interface includes four buffers: an input buffer, a receive buffer, an output buffer, and a command buffer. The input buffer contains data received from the network device and the receive buffer contains instructions for the data contained in the input buffer. The output buffer holds data to be transmitted to the network device and the command buffer includes instructions regarding transmission of the data held in the output buffer.

2. Shimojo *et al.*

Shimojo *et al.* relates to a flow control apparatus that includes a buffer and a free-buffer information cell (that indicates the amount of space available in the buffer). In one manner of flow regulation, a downstream apparatus transmits the amount of free buffer area (according to the free-buffer information cell) to an upstream apparatus. The upstream apparatus transmits cells to the downstream apparatus such that the number of cells does not exceed the amount of free buffer area indicated by the downstream apparatus.

3. Collier *et al.*

Collier *et al.* involves management of data packet transmission to a receiving buffer noting the amount of available space in the buffer. When the amount of available space in the receiving buffer is above a threshold value, then a flow control packet may be sent to a sending device that notifies the sending device of the amount of available free space in the buffer. The flow control packets are sent at predetermined time intervals.

4. Anderson

Anderson involves determining an adjusted credit value for credit buckets based on the number of time intervals elapsed since the credit bucket was last updated.

B. Rejection of Claims 8 and 25 Under 35 U.S.C. §103(a)

Claims 8 and 25 stand rejected under 35 U.S.C. §103(a) as being anticipated by Good *et al.* (US 6,240,095 B1), in view of Shimojo *et al.* (US 5,787,072). It is requested that these rejections be reversed for at least the following reason. Good *et al.* and Shimojo *et al.*, alone or in combination, do not teach or suggest all the claim limitations expressly, impliedly, or obviously.

> To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of

the teachings of the references. *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

See MPEP §706.02(j).

1. Independent Claims 8 and 25

a) Independent Claims 8 and 25 are not obvious at least because Good *et al.* and Shimojo *et al.* fail to teach or suggest a chipset and an I/O controller within the same device

In particular, independent claims 8 and 25 recite: "communicating to ***a chipset within a device coupled to the I/O controller within the device*** the amount of available memory credits" (emphasis added).

The Examiner contends that Good *et al.* teaches these aspects by equating: (1) the "I/O controller" recited in independent claims 8 and 25 with Good *et al.*'s "buffer memory interface" (item 10 of Figure 1) and (2) the "chipset" recited in independent claims 8 and 25 with Good *et al.*'s "network device" (item 12 of Figure 1) (*See* Final Office Action dated August 21, 2007, pg. 3 and Good *et al.*, Figure 1). However, this interpretation fails to teach the cited limitation because the network device is characterized as "remote," meaning that it is located in a computer that is separate from the computer that holds the buffer memory interface (*See e.g.*, "remote server" of Good *et al.*, col. 3, line 66 – col. 4, line 2). Thus, the buffer memory interface and the network device are not located within the same device. Accordingly, the network device of Good *et al.* would not be "within a device coupled to the I/O controller within the device," as recited in independent claims 8 and 25.

In response to the Appellants' arguments, the Examiner states that "Good is merely giving an example of a network device when stating at [*sic*] the network device can be a remote server. Good states that modifications and variations of the preferred embodiment are still within the scope of the invention (Good; Col 6 Lines 45-49), meaning the example given is not limiting. Nowhere does Good teach the network device being away from the network interface card as suggested by applicant" (*See* Final Office Action dated August 21, 2007, pg. 2). The Appellants respectfully disagree with such reasoning.

The Examiner does not appear to assert that the aspect of a chipset and I/O controller being in the same device is expressly taught in Good *et al.* However, an inherent teaching requires that the aspect be necessarily present in the reference.

> To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is ***necessarily present*** in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); *See* MPEP §2112(IV) (emphasis added). In view of this standard, the buffer memory interface and the network device of Good *et al.* are not necessarily present in a single device. The Examiner appears to be asserting that a modification of Good *et al.* to move the buffer memory interface and the network device to the same device would be proper to disclose the claim limitation. The Examiner points out that the illustration of the network device as a remote server was merely an example and adds that Good *et al.* does not "teach the network device being away from the network interface card" (*See* Final Office Action mailed August 21, 2007, pg. 2).

However, it does not follow that the claim limitation is **necessarily present** in the cited reference just because the cited reference fails to teach away from the claim limitation. While the identification of the "network device" as a "remote server" in Good *et al.* was presented in the form of an example (*See* Good *et al.*, Figure 1 and col. 3, line 66 – col. 4, line 2), the cited reference fails to present any other explanation or example that might indicate another specific interpretation or configuration. Although some modifications and variations of Good *et al.* may still fall within the scope of the invention, they must be apparent to those of ordinary skill in the art (*See Id.* at col. 6, ll. 46-49)—such as varying "the size of the various input, output, command and receive buffers ... according to the anticipated need for the buffer memory interface" (*See Id.* at col. 6, ll. 49-56). Good *et al.* must still teach or suggest all the claimed limitations; but based on the visual orientation of the items shown in Figure 1 (*See Id.* at Figure 1, Item 16) and the sole example specified, the cited reference is silent regarding "communicating to ***a chipset within a device coupled to the I/O controller within the device*** the amount of available memory credits" (*See* independent claims 8 and 25) (emphasis added).

The Examiner further contends, "As applicant has not defined the term 'device,' the Examiner has given the term its broadest reasonable interpretation. Using this interpretation, the whole system of Good can be considered a device" (*See* Final Office Action dated August 21, 2007, pg. 2). The Appellants respectfully aver to the contrary.

The claims must be interpreted as a whole and in light of the Specification (*See* MPEP §§2141.02, 2111). Although the Examiner should give the claims their broadest reasonable interpretation, such interpretation "must also be consistent with the interpretation that those skilled in the art would reach." *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999) *See* also MPEP §2111.

In view of a person having ordinary skill in the art, the whole system of Good *et al.*, *i.e.*, the host device, the buffer memory interface, and the network device, would not be considered one device, even under the broadest reasonable interpretation. As interpreted by a person having ordinary skill in the art, "In the context of computer technology, a device is ***a unit*** of hardware" (*See* device – a definition from Whatis.com. [Online] Available http://whatis.techtarget.com/definition/0,,sid9_gci211937,00.html, Last updated on July 25, 2001) (emphasis added) and may also be described as those units "separately installable and replaceable" (*See Id.*). Accordingly, a person having ordinary skill in the art would not consider the three items illustrated in Figure 1—"the buffer memory interface … interposed between a network device … and a host device" (*See* Good *et al.*, Figure 1 and col. 3, line 66 – col. 4, line 2)—to be one single device. Rather, they would likely be considered at least two or three separate devices (since the host device is represented by a **local computer** and the network device is represented by a **remote server**).

In response, the Examiner states that based on this definition, since a chipset and I/O controller are both units of hardware located within a "device," then the "device" of the subject claims contains multiple units of hardware (*See* Advisory Action mailed October 29, 2007, pg. 2).

The chipset and I/O controller of the subject claims are components (*e.g.*, chips) of a single computing device. These components assist in the operation of the computing device by managing data transmission within the computing device. For example, "[t]he units of a computer to which the term *device* is not applied include the motherboard, the main processor, and additional processors" (*See* device – a definition from Whatis.com. [Online] Available

http://whatis.techtarget.com/definition/0,,sid9_gci211937,00.html, Last updated on July 25, 2001) (emphasis in original). Even if a chipset and I/O controller are considered separate "devices" rather than parts, they may still be comprised within a single device because in general, "a computer can be considered a device" (*See* device – a definition from Whatis.com. [Online] Available http://whatis.techtarget.com/definition/0,,sid9_gci211937,00.html, Last updated on July 25, 2001). However, with respect to Good *et al.*, the buffer memory interface would exist on one computer and the network device/remote server would exist at another remote computer (communicating through network data, item 16 of Figure 1)—setting forth two computers. There is no reasonable manner in which the "network device" (described as a remote server) and the "buffer memory interface" communicating through network data, as situated in the orientation of Figure 1 and the corresponding description of Good *et al.*, could be interpreted as part of one single device by a person having ordinary skill in the art. Therefore, Good *et al.* fails to disclose "***communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits***" (emphasis added) as recited in independent claims 8 and 25.

The Examiner has not relied upon and the Appellants are unable to discern any part of Shimojo *et al.* that teaches the limitations discussed above. Thus, Shimojo *et al.* fails to cure the aforementioned deficiencies of Good *et al.* regarding independent claims 8 and 25. For at least these reasons, it is readily apparent that Shimojo *et al.* and Good *et al.*, alone or in combination, do not teach or suggest independent claims 8 and 25. The Appellants request that these rejections be reversed.

C. Rejection of Claims 9, 12-19, 26, and 27 Under 35 U.S.C. §103(a)

1. Claims 9, 12-19, 26, and 27

Claims 9, 12-19, 26, and 27 stand rejected under 35 U.S.C. §103(a) as being obvious over Good *et al.*, in view of Shimojo *et al.*, and further in view of Collier *et al.* (US 2002/0150049 A1). These rejections should be reversed for at least the following reason. Claims 9 and 12-19 depend from independent claim 8 and claims 26 and 27 depend from independent claim 25. The Examiner has not relied upon and the Appellants are unable to discern any part of Collier *et al.* that discloses "communicating to a chipset within a device coupled to the I/O controller within

the device the amount of available memory credits" as recited in independent claims 8 and 25. Further, claims 9, 12-19, 26, and 27 include additional limitations from independent claims 8 and 25, which were separately rejected and are thus separately patentable because the distinct rejection does not allow for these claims to stand or fall with claims 8 and 25. Therefore, Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest claims 9, 12-19, 26, and 27. Accordingly, it is respectfully requested that these rejections be reversed.

2. Claim 9

a) Claim 9 depends from patentable base claim 8

Claim 9 depends from independent claim 8 and thus incorporates the limitations thereof. The Examiner does not indicate and the Appellants do not discern any part of Collier *et al.* that cures the aforementioned deficiencies of Good *et al.* and Shimojo *et al.* with respect to independent claim 8. Therefore, Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest all the limitations of claim 9. Accordingly, the Appellants respectfully request that this rejection be reversed. Further, the Appellants believe that this claim is separately patentable for the reasons below.

b) Claim 9 is not obvious at least because Good *et al.*, Shimojo *et al.*, and Collier *et al.* fail to teach or suggest comparing each of a plurality of buffers and determining a least amount of available memory

In particular, claim 9 recites: "comparing an amount of available memory in each of a plurality of buffers contained within the I/O controller; and determining a least amount of available memory in one of the plurality of buffers to create an amount of available memory in the I/O controller." Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest this aspect.

The Examiner concedes that Good *et al.* and Shimojo *et al.* does not teach "comparing an amount of available memory in each of a plurality of buffers contained within the I/O controller" and therefore relies on Collier *et al.* at paragraph 0024, ll. 9-15 (*See* Final Office Action mailed

August 21, 2007, pg. 4). However, claim 9 recites comparing an amount of available memory in each of a plurality of buffers, *e.g.*, out of two buffers, one buffer has more available memory than the other buffer. In paragraph 0024, ll. 9-15, Collier *et al.* involves the comparison of a receiving buffer with a threshold value. The "virtual lane buffers" mentioned in paragraph 0024 refer to a set of send and receive buffers. The available space of the send buffer is not involved with any comparison. First, since the receiving buffer is compared to a threshold value and not another buffer, the cited reference does not teach or suggest comparing available memory in **each** of the buffers. Second, since the receive buffer is involved in a comparison but the send buffer is not, only **one** of the two buffers relates to a comparison aspect. It therefore cannot be said that the cited reference teaches comparing available memory in **each of a plurality of buffers** when not all the buffers of the plurality of buffers are involved in the comparison.

The Examiner does not indicate and the Appellants do not discern any part of Shimojo *et al.* and Collier *et al.* that teaches "determining a least amount of available memory in one of the plurality of buffers to create an amount of available memory in the I/O controller." Therefore, the Examiner relies on Good *et al.* at col. 5, ll. 24-31 (*See* Final Office Action mailed August 21, 2007, pg. 4). However, col. 5, ll. 24-31 of Good *et al.* discloses the indication of the size of the unused portion of an input buffer. The cited reference is silent with respect to a least amount of available memory in one of a **plurality** of buffers since only one buffer (the input buffer) is considered for memory purposes. In claim 9, for example, if there are two buffers, A and B (a plurality of buffers), and buffer A has a lesser amount of available memory than buffer B, then the amount of available memory in buffer A would be determined as the **least** amount of available memory. With just one buffer in Good *et al.*, there does not exist a **plurality** of buffers in which **one** buffer with the **least** amount of memory could be determined. Thus, Good *et al.* does not teach or suggest "determining a least amount of available memory in one of the plurality of buffers to create an amount of available memory in the I/O controller" as recited in claim 9.

In view of the foregoing, it is readily apparent that Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, fail to teach or suggest all the claim limitations of claim 9. Accordingly, claim 9 is separately patentable and it is respectfully requested that this rejection be reversed.

c) Good *et al.* is not properly combined with Collier *et al.* for the aspects of claim 9

The Appellants do not believe that the combination of Good *et al.* and Collier *et al.* is proper. To establish a *prima facie* case of obviousness, there must be a motivation to combine the teachings of Good *et al.* and Collier *et al.* found either in the references themselves or as viewed by one of ordinary skill in the art.

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, ***there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.*** Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

See MPEP §2143 (emphasis added). In addition, the combination of Good *et al.* and Collier *et al.* cannot change the principle of operation.

> If the proposed modification or combination of the prior art would ***change the principle of operation*** of the prior art invention being modified, then the teachings of the references are ***not sufficient*** to render the claims *prima facie* obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

See MPEP §2143.01(VI) (emphasis added). Claim 9 recites a comparing aspect and a determining aspect. The Examiner indicates that Collier *et al.* teaches the comparing aspect and Good *et al.* teaches the determining aspect (*See* Final Office Action mailed August 21, 2007, pg. 4). A person having ordinary skill in the art would not have the motivation to modify Good *et al.* with the aspects of Collier *et al.* Good *et al.* teaches the sending of an indication of the unused portion of an input buffer in response to a request for such information. Collier *et al.* teaches constantly monitoring a receive buffer and sending a "flow control packet" when the amount of available free space exceeds a predetermined threshold value. In Good *et al.*, the receiver of such a "flow control packet" would not be configured to receive this extra information that it did not request. Further, the network interface circuit of Good *et al.* would have to be altered to have constant buffer monitoring capabilities. The principle of operation of Good *et al.* would need to

be altered to accommodate such a change, which is improper according to MPEP §2143.01(VI).

Therefore, the Examiner has failed to establish that Good *et al.* and Collier *et al.* are properly combinable. The Appellants respectfully request that the obviousness rejection be reversed.

3. Claim 14

a) Claim 14 depends from claim 13, which depends from claim 12, which depends from claim 9, which depends from patentable base claim 8

Claim 14 depends from claim 13, which depends from claim 12, which depends from claim 9, which depends from independent claim 8, thus incorporating the limitations thereof. The Examiner does not indicate and the Appellants do not discern any part of Collier *et al.* that cures the aforementioned deficiencies of Good *et al.* and Shimojo *et al.* with respect to independent claim 8. Therefore, Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest all the limitations of claim 14. Accordingly, the Appellants respectfully request that this rejection be reversed. Further, the Appellants believe that this claim is separately patentable for the reasons below.

b) Claim 14 is not obvious at least because Good *et al.*, Shimojo *et al.*, and Collier *et al.* fail to teach or suggest temporarily storing data sent from the chipset in a plurality of buffers

In particular, claim 14 recites: "wherein temporarily storing the data [sent from the chipset in the I/O controller] in at least one buffer comprises: storing the data in a ***plurality of buffers***" (emphasis added). Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, fail to teach or suggest this aspect.

The Examiner does not indicate and the Appellants do not discern any part of Good *et al.* or Shimojo *et al.* that discloses this aspect. The Examiner contends that Collier *et al.* teaches this

aspect at Figure 3, item 322, paragraph 0030, ll. 4-7, and paragraph 0033, ll. 1-7 (*See* Final Office Action mailed August 21, 2007, pg. 5). The Appellants respectfully disagree.

The Appellants note that Figure 3 does not include an item 322. Figure 3 illustrates a flow chart of determining available space in a buffer. Paragraph 0030, ll. 4-7 describes an indication of the amount of space available in an 8K buffering device as a function of time (clock cycles). In paragraph 0033, ll. 1-7, Collier *et al.* utilizes two pointers, one being a read pointer indicating the first position of the buffer available to store data and the other being a write pointer indicating the first position of the same buffer from which data will be output. However, the cited reference only provides for **one** buffer at the receiving device. Therefore, Collier *et al.* does not teach or suggest temporarily storing data received from a chipset in a **plurality of buffers**.

In view of the above, the Appellants respectfully submit that Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest all the limitations of claim 14. This claim is separately patentable and it is respectfully requested that this rejection be reversed.

4. Claim 17

a) Claim 17 depends from claim 16, which depends from claim 15, which depends from claim 13, which depends from claim 12, which depends from claim 9, which depends from patentable base claim 8

Claim 17 depends from claim 16, which depends from claim 15, which depends from claim 13, which depends from claim 12, which depends from claim 9, which depends from independent claim 8, thus incorporating the limitations thereof. The Examiner does not indicate and the Appellants do not discern any part of Collier *et al.* that cures the aforementioned deficiencies of Good *et al.* and Shimojo *et al.* with respect to independent claim 8. Therefore, Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest all the limitations of claim 17. Accordingly, the Appellants respectfully request that these rejections be reversed. Further, the Appellants believe that this claim is separately patentable for the reasons below.

b) Good *et al.* is not properly combined with Collier *et al.* for the aspects of claim 17

The Appellants do not believe that the combination of Good *et al.* and Collier *et al.* is proper. To establish a *prima facie* case of obviousness, there must be a motivation to combine the teachings of Good *et al.* and Collier *et al.* found either in the references themselves or as viewed by one of ordinary skill in the art (*See* MPEP §2143). Further, the Examiner as factfinder must provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (*See* MPEP §2141, *KSR*, 550 U.S. 82, USPQ2d at 1396). This includes some explanation of the rationale used to combine the cited references to teach the subject claims. The Examiner has not provided such explanation. As noted above in the discussion regarding claim 9, Good *et al.* and Collier *et al.* are not properly combinable because the principle of operation of Good *et al.* would need to be altered to accommodate the changes of Collier *et al.*, which is improper according to MPEP §2143.01(VI). Accordingly, this claim is separately patentable; reconsideration and reversal of this rejection is respectfully requested.

5. Claims 19 and 27

a) Claim 19 depends from claim 18, which depends from claim 15, which depends from claim 13, which depends from claim 12, which depends from claim 9, which depends from patentable base claim 8; claim 27 depends from claim 26, which depends from patentable base claim 25

Claim 19 depends from claim 18, which depends from claim 15, which depends from claim 13, which depends from claim 12, which depends from claim 9, which depends from independent claim 8, and claim 27 depends from claim 26, which depends from independent claim 25, thus incorporating the limitations thereof. The Examiner does not indicate and the Appellants do not discern any part of Collier *et al.* that cures the aforementioned deficiencies of Good *et al.* and Shimojo *et al.* with respect to independent claims 8 and 25. Therefore, Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest all the

limitations of claims 19 and 27. Accordingly, the Appellants respectfully request that these rejections be reversed. Further, the Appellants believe that these claims are separately patentable for the reasons below.

b) Claims 19 and 27 are not obvious at least because Good *et al.*, Shimojo *et al.*, and Collier *et al.* fail to teach or suggest simultaneously keeping track of the amounts of memory credits being emptied from, received by, and distributed to buffers at the I/O controller

In particular, claims 19 and 27 recite: "***simultaneously*** keeping track of amounts of memory credits the I/O controller empties onto the I/O bus, amounts of memory credits sent to the I/O controller and amounts of memory credits made available by distribution of data sent from the chipset to a plurality of buffers contained within the I/O controller" (emphasis added) or analogous aspects. Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, fail to teach or suggest this aspect.

The Examiner does not indicate and the Appellants do not discern any part of Shimojo *et al.* or Collier *et al.* that teaches this aspect. The Examiner contends that Good *et al.* discloses the simultaneous tracking of: amounts of memory credits the I/O controller empties onto the I/O bus at col. 6, ll. 10-14, amounts of memory credits sent to the I/O controller at Figure 3, item 60 and col. 5, line 66 – col. 6, line 4, and amounts of memory credits made available by distribution of data sent from the chipset to a plurality of buffers contained within the I/O controller at Figure 1, item 74 and col. 5, ll. 30-32 (*See* Final Office Action mailed August 21, 2007, pg. 6). The Appellants respectfully aver to the contrary.

In col. 6, ll. 10-14, Good *et al.* describes updating a credit register 74 based on how much an input buffer (containing data received from the network device 12) has been cleared. However, Good *et al.* is silent regarding emptying memory credits onto an **I/O bus**. Rather, the cited passage indicates that data contained in an input buffer has been cleared. Therefore, this passage does not teach or suggest tracking "amounts of memory credits the I/O controller empties onto the I/O bus."

In Figure 3, item 60 and col. 5, line 66 – col. 6, line 4, Good *et al.* discloses data being transmitted from the host device 14 to the network device 12, in which the word count 60 of the data in combination with flags indicate whether the transmission is complete so as to determine

whether the connection for data should remain open. The cited portions do not indicate that "***amounts*** of memory credits sent to the I/O controller" (emphasis added) are tracked, but instead indicates that a connection to the network device 12 is held open until there is an indication that transmission of a packet of data to the network device 12 is complete.

Figure 1, item 74 and col. 5, ll. 30-32 of Good *et al.* notes that the credit register 74 stores the size of the unused portion of the input buffer (containing data received from the network device 12). While the buffer memory interface includes four buffers (*i.e.*, input buffer, receive buffer, output buffer, and command buffer), when the buffer memory interface receives data from the network device, it writes that incoming data to the input buffer only. Since the incoming data appears to be written to just a single buffer, Good *et al.* does not teach or suggest a distribution of data received by the I/O controller from the chipset to a "***plurality*** of buffers contained within the I/O controller" (emphasis). Accordingly, the "amounts of memory credits made available" by this distribution is also not described in the cited reference.

Further, Good *et al.* fails to note the nature of the tracking as **simultaneous.** The subject claims provide for a **simultaneous** tracking of memory credits in three distinct aspects, while even if the cited reference disclosed all three aspects, it is silent regarding their simultaneous timing.

In view of the foregoing, it is readily apparent that Good *et al.*, Shimojo *et al.*, and Collier *et al.*, alone or in combination, do not teach or suggest all the claim limitations, namely, "***simultaneously*** keeping track of amounts of memory credits the I/O controller empties onto the I/O bus, amounts of memory credits sent to the I/O controller and amounts of memory credits made available by distribution of data sent from the chipset to a plurality of buffers contained within the I/O controller" (emphasis added) as recited in claims 19 and 27. These claims are separately patentable and it is respectfully requested that these rejections be reversed.

D. Rejection of Claims 10 and 11 Under 35 U.S.C. §103(a)

1. Claims 10 and 11

Claims 10 and 11 stand rejected under 35 U.S.C. §103(a) as being obvious over Good *et al.*, in view of Shimojo *et al.*, and further in view of Collier *et al.* and Anderson (US 2003/0223369 A1). It is requested that this rejection be reversed for at least the following

reason. Claims 10 and 11 depend from independent claim 8. The Examiner has not relied upon and the Appellants are unable to discern any part of Anderson that cures the aforementioned deficiencies regarding independent claim 8. Further, claims 10 and 11 include additional limitations from independent claim 8, which were separately rejected and are thus separately patentable because the distinct rejection does not allow for these claims to stand or fall with claim 8. Thus, it is readily apparent that Good *et al.*, Shimojo *et al.*, Collier *et al.*, and Anderson, alone or in combination, do not teach or suggest claims 10 and 11; the Appellants request that these rejections be reversed.

For the reasons set forth above, the Appellants respectfully request the Board overturn the rejection of claims 8-19 and 25-27.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

Lori A. Ciccio 1/25/08
Date

VIII. CLAIMS APPENDIX

The claims involved in this Appeal are as follows:

1. (Withdrawn) An apparatus comprising:

credit management logic to communicate to a chipset an available amount of memory credits in an input/output (I/O) controller;

a first buffer of a first memory size contained within the I/O controller coupled to, and in communication with the credit management logic; and

a second buffer of a second memory size contained within the I/O controller coupled to, and in communication with the credit management logic.

2. (Withdrawn) The apparatus of claim 1, wherein the first buffer and the second buffer are the same size.

3. (Withdrawn) The apparatus of claim 2, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

4. (Withdrawn) The apparatus of claim 1, wherein the first buffer and the second buffer are different sizes.

5. (Withdrawn) The apparatus of claim 4, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

6. (Withdrawn) The apparatus of claim 1, further comprising:

a transaction layer containing the credit management logic; and

an internal switch to divide data received from the chipset between one of the first buffer, the second buffer and both the first and second buffers.

7. (Withdrawn) The apparatus of claim 1, wherein the I/O controller is one of a bridge, a switch, an endpoint and a root complex.

8. (Previously Presented) A method comprising:

determining an amount of available memory credits in an input/output (I/O) controller;

communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits; and

sending an amount of data from the chipset to the I/O controller, the amount of data sent being one of equivalent to or less than the communicated available memory credit amount.

9. (Original) The method of claim 8, wherein determining the available amount of memory credits comprises:

comparing an amount of available memory in each of a plurality of buffers contained within the I/O controller; and

determining a least amount of available memory in one of the plurality of buffers to create an amount of available memory in the I/O controller.

10. (Original) The method of claim 9, further comprising:

converting the amount of available memory in the I/O controller to an amount of available memory credits.

11. (Original) The method of claim 10, wherein converting the amount of available memory to an amount of available memory credits comprises:

dividing the available amount of memory in the I/O controller by an amount of memory equivalent to one credit.

12. (Original) The method of claim 9, further comprising:

temporarily storing the data sent from the chipset in the I/O controller.

13. (Original) The method of claim 12, wherein temporarily storing the data comprises:

temporarily storing the data in at least one buffer contained within the I/O controller.

14. (Original) The method of claim 13, wherein temporarily storing the data in at least one buffer comprises:

storing the data in a plurality of buffers.

15. (Original) The method of claim 13, further comprising:

emptying the buffer of at least some of the data temporarily stored in the I/O controller to create a new amount of available memory credits in the I/O controller.

16. (Original) The method of claim 15, wherein emptying at least some of the data comprises:

sending the data to at least one I/O bus coupled to the I/O controller.

17. (Original) The method of claim 16, wherein sending the data to at least one I/O bus comprises:

sending the data to a plurality of I/O buses coupled to the I/O controller.

18. (Original) The method of claim 15, further comprising:

keeping track of the number of available memory credits in the I/O controller.

19. (Original) The method of claim 18, wherein keeping track of the number of memory credits comprises:

simultaneously keeping track of amounts of memory credits the I/O controller empties onto the I/O bus, amounts of memory credits sent to the I/O controller and amounts of memory credits made available by distribution of data sent from the chipset to a plurality of buffers contained within the I/O controller.

20. (Withdrawn) A system comprising:

a peripheral component interconnect (PCI) link;

a first input/output (I/O) bus;

a second I/O bus; and

an I/O controller coupled to the PCI link, the first I/O bus and the second I/O bus, the I/O controller comprising:

credit management logic to communicate to the PCI link an available amount of memory credits in the I/O controller,

a first buffer of a first memory size coupled to and in communication with the credit management logic, the PCI link and the first I/O bus, and

a second buffer of a second memory size couple to and in communication with the credit management logic, the PCI link and the second I/O bus.

21. (Withdrawn) The system of claim 20, wherein the first buffer and the second buffer are the same size.

22. (Withdrawn) The system of claim 21, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

23. (Withdrawn) The apparatus of claim 20, wherein the first buffer and the second buffer are different sizes.

24. (Withdrawn) The apparatus of claim 23, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

25. (Previously Presented) A machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising:

determining an amount of available memory credits in an input/output (I/O) controller;

communicating to a chipset within a device coupled to the I/O controller within the device the amount of available memory credits; and

sending an amount of data from the chipset to the I/O controller, the amount of data sent being one of equivalent to or less than the communicated available memory credit amount.

26. (Original) The machine readable medium of claim 25, wherein determining the available amount of memory credits comprises:

comparing an amount of available memory in each of a plurality of buffers contained within the I/O controller; and

determining a least amount of available memory in one of the plurality of buffers to create an amount of available memory in the I/O controller.

27. (Original) The machine read medium of claim 26, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

temporarily storing the data in at least one buffer contained within the I/O controller;

emptying the buffer of at least some of the data temporarily stored in the I/O controller onto an I/O bus coupled to the I/O controller to create a new amount of available memory credits in the I/O controller; and

simultaneously tracking amounts of memory credits the I/O controller empties onto the I/O bus, amounts of memory credits sent to the I/O controller from the chipset and amounts of memory credits made available by distribution of the data sent from the chipset to a plurality of buffers contained within the I/O controller.

IX. EVIDENCE APPENDIX

No evidence is submitted with this appeal.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings exist.